IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	
	:	Examiner:
Anne KASZYNSKI & Jacques ABILY	:	
	::	
Serial No.: To be assigned.	:	Group Art Unit:
	:	
Filed: Concurrently herewith	:	Corresponding to:
	:	French Patent
	:	Application FR 02 09691
For: **Procédé de vérification fonctionnelle d'un modèle de circuit intégré pour constituer une plate-forme de vérification, équipement émulateur et plate-forme de vérification.** English title (when application is translated) Method for Functional Verification of an Integrated Circuit Model in Order to Create a Verification Platform, Equipment Emulator and Verification Platform	:	Dated July 30, 2002

McLean, Virginia

CLAIM FOR BENEFIT OF FILING DATE
OF PRIOR FOREIGN APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In the matter of the above-identified application, a claim is hereby made under the provisions of 35 U.S.C. 119 for the benefit of the filing date of the corresponding French application No 02/09691 filed July 30, 2002, which is referred to in the Declaration of the present case.

A certified copy of said French application will be forwarded as soon as it is available.

Respectfully submitted,

MILES & STOCKBRIDGE P.C.

Date July 28, 2003

By: Edward J. Kondracki
Edward J. Kondracki
Registration No. 20,604

Miles & Stockbridge, P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
Tel.: (703) 903-9000